24

IN THE MATTER OF
KOREAN PATENT APPLICATION
UNDER SERIAL NO. 6441/1993

I, THE UNDERSIGNED, HEREBY DECLARE :
THAT I AM CONVERSANT WITH BOTH THE KOREAN AND THE ENGLISH LANGUAGES : AND

THAT I AM A COMPETENT TRANSLATOR OF THE APPLICATION PAPERS THE PARTICULARS OF WHICH ARE SET FORTH BELOW :

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IN THE NAME OF: GOLDSTAR CO., LTD.

FOR: APPARATUS FOR CONTROLLING RECORDING AND REPRODUCTION IN DICITAL VIDEO CASSETTE TAPE RECORDER

IN WITNESS WHEREOF, I SET MY HAND HERETO

THIS 13TH DAY OF OCTOBER, 2001

BY _____

YEON JEONG KIM

[Translation]

PATENT APPLICATION

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Title of the invention : APPARATUS FOR CONTROLLING RECORDING AND REPRODUCTION IN DIGITAL VIDEO CASSETTE TAPE RECORDER

This application is hereby filed pursuant to Article 42 of the Patent Law.
This 16th day of April, 1993
/S/ Attorney : Jang Won PARK

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* Encls.

[Translation]

SPECIFICATION

1. Title of the Invention

APPARATUS FOR CONTROLLING RECORDING AND REPRODUCTION IN DIGITAL VIDEO CASSETTE TAPE RECORDER

2. Brief description of the Drawings

Figure 1 is a block diagram of a conventional recording circuit for a digital VCR.

Figure 2 is a block diagram of a conventional reproduction circuit for a digital VCR.

Figure 3 is a schematic view illustrating recording tracks of a magnetic tape and a trace of heads travelling in a speed-varied reproduction mode in accordance with the prior art.

Figure 4 is a schematic view illustrating a correlation among frames in accordance with a video compression system.

Figure 5 is a schematic view illustrating an encoded bit stream.

Figure 6 is a schematic view illustrating synchronous blocks of a video signal for recording and reproduction.

Figure 7 is a block diagram of a recording control circuit for a digital VCR in accordance with the present invention.

Figure 8 is a block diagram of a reproduction control circuit for a digital VCR in accordance with the present invention.

Figure 9 is a schematic view illustrating recording tracks in accordance with the

present invention.

Figure 10 is a waveform diagram of signals generated in recording position control in Figure 7.

Figure 11 is a schematic view illustrating recording position-synchronized blocks in accordance with the present invention in Figure 7.

Figure 12 is a flow chart illustrating a frame detection procedure in accordance with the present invention.

Figures 13 illustrates a capstan servo speed control in accordance with the present invention.

Figure 14 is a waveform diagram of signals generated in frame removal in Figure 8.

**** Explanation for the major reference numerals ****

18: digital recording unit	19: frame position information recording unit
20: frame extracting unit	21: frame recording position controlling unit
32: digital reproduction unit	33: frame position information detecting unit
34: tape speed controlling unit	35: frame removing unit
M_1: drum motor	M_2: capstan motor

3. Detailed description of the present invention

The present invention relates to recording and reproduction of digital signals of a digital VCR and particularly, to a circuit for controlling recording and reproduction in a digital cassette tape recorder capable of separating specific data for speed-varied reproduction from compressed digital video signals and recording them on designated tracks in a recording mode, recording position information of the designated tracks on a control

track by an index head or recording position information of recording position-synchronized blocks at the starting portions of the designated tracks recorded with the specific data so as to accurately scan the designate tracks in a reproduction mode, controlling a capstan servo speed so as to maintain the travel of a magnetic tape at a normal speed and periodically or non-periodically accelerate or decelerate it in case of speed-varied mode, thereby making heads travel repeatedly at the normal speed and the high speed. Accordingly, the present invention provides a repeatability of reproduced video at a varied speed without any deterioration in picture quality in that it enables recording of specific data for speed-varied reproduction and continuous detection of the specific data in the speed-varied reproduction.

Generally, for analog/digital conversion for converting an analog video signal into a digital video signal and linear quantization, a signal transmission rate of about 100 Mega bits per second is typically required in the case of normal TV broadcast signal such as NTSC, SECAM and PAL signals. On the other hand, high definition TV (HDTV) signal with higher resolution than that of the normal TV broadcast signal requires a signal transmission rate higher than 100 Mega bits.

For achieving data transmission in a limited transmission band, digitalized video signals should be transmitted in the form compressed in accordance with the video data compression technique.

In case of digital cassette tape recorders (digital VCRs) having a limitation on record bandwidth, signals recorded on a magnetic tape may be digital, normal TV signals having the form of compressed signals or digital, HDTV signals having the form of compressed signals.

Referring to Figure 1, there is illustrated a conventional recording circuit for a digital VCR. As shown in Figure 1, the recording circuit includes an interface 1 for converting a compressed digital video signal into a signal having the recordable form, an interleaving and

channel-dividing circuit 2 for interleaving an output V1 from the interface 1 in a predetermined form to reduce burst error and channel-dividing it to be matched with the zero bandwidth of a recording channel, recording formatters 3A and 3B for respectively converting outputs V2 and V3 of the interleaving and channel-dividing circuit 2 to record formats each including a synchronous signal, an identification signal and redundancy bits for error correction codes, channel modulators 4A and 4B for modulating outputs V6 and V7 of the channel modulators 4A and 4B for modulating outputs V4 and V5 of the recording formatters 3A and 3B, respectively, recording amplifiers 5A and 5B for amplifying outputs V6 and V7 of the channel modulators 4A and 4B to a certain level, respectively, a drum pulse generator 7 for outputting two pulses at every rotation of a head drum 6 caused by driving of a drum motor M1, and switches SW1 and SW2 for performing their switching operations based on output SWP from the drum pulse generator 7 to selectively transmit outputs V8 and V9 of the recording amplifiers 5A and 5B to heads HD1 (or HD3) and HD2 (or HD4), respectively. In Figure 1, the reference numeral 8 denotes a guide pin, 10 a pinch roller, and 9 a capstan adapted to be rotated by a capstan motor M1.

Figure 2 is a block diagram illustrating the conventional reproduction circuit for the digital VCR. As shown in Figure 2, the reproduction circuit includes reproduction amplifiers 11A and 11B for receiving outputs from selected heads HD1 (or HD3) and HD2 (or HD4) mounted on the head drum 6 via the switches SW1 and SW2 switched in accordance with the output SWP from the drum pulse generator 7 and amplifying them, respectively, equalizers 12A and 12B for compensating distortions of frequency characteristics of outputs V10 and V11 of the reproduction amplifiers 11A and 11B, respectively, channel demodulators 13A and 13B for demodulating outputs V12 and V13 of the equalizers 12A and 12B, respectively, sync-detecting and error-correcting circuits 14A and 14B for detecting synchronous signals SYNC added in a recorded signal from the outputs V14 and

V15 of the channel demodulators 13A and 13B and correcting errors of the outputs V14 and V15, respectively, deinterleaving circuits 15A and 15B for deinterleaving outputs V16 and V17 of the sync-detecting and error-correcting circuits 14A and 14B into the original signal form, respectively, a deformatter 16 for recovering outputs V18 and V19 of the deinterleaving circuits 15A and 15B to the original signal format, and an interface 17 for converting an output V20 of the deformatter 16 into a reproduced digital signal V0 and outputting it.

Now, operations of the conventional circuits will be described in conjunction with Figures 3 to 6.

First, in a recording mode, a compressed HDTV signal or compressed normal TV signal is applied to the interface 1 which, in turn, converts the received signal into signal V1 capable of being recorded and reproduced. The signal V1 is then interleaved into a predetermined form to reduce burst errors through the interleaving and channel-dividing circuit 2 and channel-divided so as to be matched with the bandwidth of the recording channel.

The outputs V2 and V3 from the interleaving and channel-dividing circuit 2 are applied to the recording formatters 3A and 3B and then added with synchronous signals SYNC, identification signals ID and redundancy bits for error correction in the recording formatters 3A and 3B as shown in Figure 6. Resultant signals from the recording formatters 3A and 3B are then received in the channel modulators 4A and 4B matched with a predetermined recording format, respectively.

The outputs V6 and V7 from the channel modulators 4A and 4B are applied to the recording amplifiers 5A and 5B which, in turn, amplify them, respectively.

In this case, the drum pulse generator 7 generates two pulses at every rotation of the head drum 6 driven by the drum motor M1.

At this time, the video tape in gear with the capstan 9 and the pinch roller 10 has a rolling angle of over 180° at the head drum 6 by the guide pin 8. As the capstan motor M2 rotates the capstan 9, the speed of transmission is determined and the outputs V8 and V9 of the recording amplifiers 5A and 5B are switched by the output SWP of the drum pulse generator 7 at the switches SW1 and SW2.

Accordingly, the outputs V8 and V9 of the recording amplifiers 5A and 5B are allowed to the heads HD1 (or HD3) and HD2 (or HD4) through the switches SW1 and SW2 thus to be recorded in the video tape in the same recording format as shown in Figure 3. Meanwhile, frames have a mixed form of intra-frames (I-frames) able to be independently decoded as shown in Figure 4 and predictive frames (P-frames) compressed by moving information of previous screen and disable to be independently decoded, in accordance with a video compression system for HDTV signals or an MPEG (Moving Picture Experts Group) system. Bit rate generated in each frame is non-uniform, as shown in Figure 5.

In a reproduction mode, the magnetic tape travels by the rotation of the capstan 9 and the pinch roller 10 caused by the capstan motor M2 while being in contact with the head drum 6 rotating by the driving force of the drum motor M1. At this time, the heads HD1 (or HD3) and HD2 (or HD4) detect signals on the magnetic tape and send then to the reproduction amplifiers 11A and 11B via the switches SW1 and SW4 switched by the output SWP of the drum pulse generator 7, respectively.

The signals received in the reproduction amplifiers 11A and 11B are amplified to a predetermined level and then sent to the equalizers 12A and 12B which, in turn, outputs signals V12 and V13 having compensated frequency characteristics, respectively. The signals V12 and V13 from the equalizers 12A and 12B are then applied to the channel demodulators 13A and 13B, respectively, so as to be demodulated.

Outputs V14 and V15 from the channel demodulators 13A and 13B are received in

examples given.

Figure 7 is a block diagram of a recording control circuit for a digital VCR in accordance with the present invention. As shown in Figure 7, the recording control circuit for the digital VCR comprises a digital recording unit 18 which comprises an interleaving and channel-dividing circuit 2, recording formatters 3A and 3B, channel-dividing modulators 4A and 4B, recording amplifiers 5A and 5B, a head drum 6 equipped with heads HD1 to HD4, a drum pulse generator 7 and switches SW1 and SW2, a frame extracting unit 20 which comprises a buffer 22 adapted to buffer the output signal V1 of the interface 1 and thereby amplify it to a predetermined level, a frame detector 24 adapted to detect specific data corresponding to an intra-frame and a frame memory 23 adapted to store the detected specific data, a frame recording position controlling unit 21 which comprises a track number calculator 28 adapted to calculate the number of tracks, a multiplexing timing generator 27 adapted to operate an output SWP of the drum pulse generator 7 and thereby generate an output SWP of the drum pulse generator 7 and thereby generate a multiplexing timing signal V27, a bit stuffing circuit adapted to make the output signal V23 of the frame memory 23 have a constant data length when the output signal V23 is at an underflow state and a multiplexer 25 adapted to multiplex the output signals V22 and V23 of the frame extracting unit 20 and thereby output a signal V25 and a frame position information recording unit 19 which comprises a frame position recorder 29 adapted to receive the multiplexing timing signal V27' from the frame recording position controlling unit 21 and record on the leading portion of a track for varied speed, position information of a next track for speed change and an index signal recorder 30 adapted to record index information of a track to be scanned by an index head 31.

Figure 8 is a block diagram of the reproduction control circuit for the digital VCR

in accordance with the present invention. As shown in Figure 8, the reproduction control circuit comprises a digital reproduction unit 32 comprises the head drum 6 equipped with the heads HD1 to HD4, the drum pulse generator 7, switches SW3 and SW4, reproduction amplifiers 11A and 11B, equalizers 12A and 12B, channel demodulators 13A and 13B and sync-detecting and error-correcting circuit 14A and 14B, a frame position information detecting unit 33 which comprises an index signal detector 36 adapted to detect index information, a recording position-synchronized block detector 40 adapted to detect, from the outputs V16 and V17 of the synch-detecting and error-correcting units 14A and 14B, position information of a specific track including specific data recorded and a recording position decoder 39 adapted to decode the detected position information, a tape speed controlling unit 34 which comprises a capstan servo-speed calculating circuit 38 adapted to operate outputs V36 and V39 of the frame position frame position frame detecting unit 33 and a drive signal generator 37 adapted to generate a drive signal V37 for controlling the speed of the capstan motor M2 and a frame removing unit 35 which includes a frame removal timing generator 41 adapted to operate an output of the drum pulse generator 7 and outputs V36 and V39' of the frame position information detecting unit 33 and thereby generate a timing signal for removing specific data for speed-varied reproduction, a stuffing bit-detecting and removing circuit 42 adapted to detect and remove a stuffing bit added for preventing generating of the underflow of the frame memory 23 and a deformatter 16 adapted to convert an output of the digital reproduction unit 32 to the format having the signal form prior to the record. Reference numeral 8 designates a guide pin, 9 a capstan, 10 a pinch roller and M1 a drum motor.

Operations of the apparatus for controlling recording and reproduction in the digital VCR in accordance with the present invention will be described, in conjunction with Figures 4 to 6 and 9 to 14.

First, in a recording mode, an input signal V1 such as a compressed HDTV signal or compressed normal TV signal is applied to the interface 1 which, in turn, converts the received signal into a signal V1 having the form capable of being recorded and reproduced. The signal V1 from the interface 1 is then applied to the frame extracting unit 20. In the frame extracting unit 20, the received signal V1 is buffered and amplified by the buffer 22. By the buffering and amplifying operations, the signal V1 is delayed for a predetermined time. The frame detector 24 detects compressed I-frames repeated at intervals of n frames, from a bit stream encoded to have frames with different compressed bit lengths. The frame memory 23 stores data of the detected I-frames.

In other words, compressed digital data of the I-frames repeatedly present at intervals of n frames are separated from the encoded bit stream shown in Figure 4 and then duplicatively recorded on a specific track because they can be independently decoded. A write enable signal W/E of high level is applied to the frame memory 23 only for the period of detecting I-frames from the encoded bit stream by the frame detector 24. As a result, the frame memory 23 can store only the compressed video data of the I-frames.

This procedure for detecting I-frames will be described in detail, in conjunction with Figure 12. An input bit stream is received in the frame detector 24 and then decoded. The frame detector 24 detects a frame mark code from a header of each frame in the bit stream. When the frame mark code is detected, an increment in frame counted value is carried out. Where I-frames are present at intervals of n frames, the number of counted frames is compared with the number of repeated I-flames. When a 2K-th frame mark code (K = 0, 1 , 2, $\cdots\cdots$) is detected by the comparison, a write enable signal W/E of high level is applied to the frame memory 23, thereby enabling compressed digital data bits of a corresponding I-frame to be stored . When a next frame mark code is detected, a

write enable signal W/E of low level is applied to the frame it is possible to prevent frames of the frame bit stream other than I-frames from being stored.

At this time, the frame recording position controlling unit 21 sends selectively I-frame data V23 and record data V22 outputted from the frame extracting unit 20 to the digital recording unit 18 at a predetermined timing. Accordingly, a recording format shown in Figure 9 is formed in the digital recording unit 18. On the other hand, since lengths of compressed data of frames are non-uniform, the frame memory 23 may encounter an underflow phenomenon that data stored in the frame memory 23 at the moment an I-frame is recorded in the frame memory 23 is insufficient or an overflow phenomenon that data stored in the frame memory 23 prior to recording of an I-frame is full.

At this time, assuming that the average bit rate of input data received in the interface 1 is R and the size of regions of the input data occupied by I-frames is a, the average bit rate of data to be recorded is expressed by R + aR. This average bit rate of data is calculated in the track number calculator 28.

In this case, a can be calculated from a = the number of tracks, i, for I-frames/ the number of tracks, j, for P-flames. Here, the number of tracks, i, is generally determined by the average bit rate of I-frames.

The multiplexing timing generator 27 operates an output V28 of the track number calculator 28 which calculates the number of tracks, i, and the number of tracks, j. The multiplexing timing generator 27 also operates the output SWP of the drum pulse generator 7. By these operations, a reference pulse is calculated. One pulse of the output SWP of the drum pulse generator 7 corresponds to a recording period for one track in a case of recording one-channel data and to a recording period for two tracks in a case of recording two-channel data. Accordingly, the multiplexing timing generator 27 outputs a

switching signal V27 enabling the multiplexer 25 to selectively output data V23 for double speed stored in the frame memory 23 and normally-recorded data (Figure 10B) buffered and amplified by the buffer 22, as shown in Figure 10D.

At this time, in the output V22 from the buffer 22 shown in Figure 10B Δt represents the period for delaying outputting of I-frames present between the first recording track and a predetermined track so as to prevent an underflow phenomenon. In the worst case where an underflow phenomenon occurred in the frame memory 23, the bit stuffing unit 26 performs a bit stuffing operation for adding, to data of I-frames, escape synchronous codes and dummy bits capable of being detected in reproduction, so as to make the data have a constant length. On the other hand, where an overflow phenomenon occurred in the frame memory 23, a write enable signal W/E of low level is set from the frame detector 24 to the frame memory 23 for a predetermined period.

Also, in the frame position information recording unit 19 received the output V27'of the multiplexing timing generation unit 27 in the frame recording position controlling unit 21, the frame position recorder 29 and the index signal recorder 30 receive the output V27' from the multiplexing timing signal generator 27 of the frame recording position controlling unit 21. As shown in Figure 8, the frame position recorder 29 outputs information V29 based on its frame position discrimination to the recording formatters 3A and 3B. Based on the information V29, the recording formatters 3A and 3B form a synchronous block including information indicative of the position of a track including a next I-frame recorded, in each video data region. Here, the recording position information represents the code converted from the number of tracks present between the track including the current I-frame recorded and the track including the next I-frame recorded, as shown in Figure 11.

On the other hand, the index signal recorder 30 outputs index information V30

by receiving the output V27 of the multiplexing generation unit 27, namely, a pulse indicative of whether an I-frame has been recorded or not, to the index head 31 which, in turn, records the index information V30 on a control track as shown in Figure 9.

Namely, the above-mentioned overall operations will be described in detail. As the head drum 6 carrying the heads HDI to HD4 is rotated by the driving force of the drum motor Ml while the magnetic tape engaged between the capstan 9 and the pinch roller 10 is fed by the driving force of the capstan motor M2, the interface 1 receiving the input signal V1 such as the compressed HDTV signal or the normal TV signal applies its output V1 to the frame extracting unit 20. Thereafter, the recorded data is buffered and amplified in the buffer 22 for a predetermined period while the I-frame data is stored in the frame memory 23 in accordance with the write enable signal W/E from the frame detector 24.

Subsequently, the multiplexer 25 receives selectively the output V22 from the buffer 22 and the output V23 from the frame memory 23, based on the output V27 from the multiplexing timing generator 27. As a result, the multiplexer 25 outputs the output signal V25 shown in Figure 10 to the digital recording unit 18. Thereafter, the interleaving and channel-dividing circuit 2 of the digital recording unit 18 interleaves the signal V25 to a predetermined form for reducing burst errors and then outputs signals V2 and V3 channel-divided to be matched with a recording channel bandwidth, to the recording formal tars 3A and 3B, respectively.

Accordingly, the recording formatters 3A and 3B form synchronous blocks shown in Figure 6 so as to add synchronous signals SYNC, identification signals ID and error correction codes ECC. The recording formatters 3A and 3B also form position information blocks of recording tracks, based on the output V29 from the frame position recorder 29 in the frame position information recording unit 19, thereby forming position

information about the first synchronous blocks of the tracks including I-frames recorded.

Outputs V4 and V5 are converted to a predetermined recording format in the channel modulators 4A and 4B, amplified to a predetermined level by the recording amplifiers 5A and 5B, and then selectively sent to the heads HD1 (or HD3) and HD2 (or HD4) via the switches SW1 and SW2 switched by the output SWP of the drum pulse generator 7 generated by the rotation of the drum motor M1.

Thus, the outputs of the recording amplifiers 5A and 5B selectively applied to the heads HD1 (or HD3) and HD2 (or HD4) via the switches SW1 and SW2 being switched are recorded on the magnetic tape in a recording format shown in Figure. 9.

On the other hand, when a speed-varied reproduction mode is selected in a case that data of the recording format shown in Figure 9 has been recorded on the magnetic tape, the data recorded on the magnetic tape is reproduced in the digital reproduction unit 32. That is signals recorded on the magnetic tape are detected by the heads HD1 (or HD3) and HD2 (or HD4) while the magnetic tape engaged between the capstan 9 and the pinch roller 10 rotated by the capstan motor M2 travels on the head drum 6 driven by the drum motor Ml.

The signals detected by the heads HDI (or HD3) and HD2 (or HD4) are sent to the reproduction amplifiers 11A and 11B via the switches SW3 and SW4 switched by the output SWP of the drum pulse generator 7, respectively. The signals received in the reproduction amplifiers 11A and 11B are amplified to a predetermined level and then sent to the equalizers 12A and 12B which, in turn, compensate distortions of frequency characteristics of the amplified signals V10 and V11, respectively. Resultant signals Vl2 and Vl3 from the equalizers 12A and 12B are then applied to the channel demodulators 13A and 13B which, in turn, demodulate the output signals Vl2 and Vl3 to the original signal forms, respectively.

Output signals Vl4 and Vl5 from the channel demodulators 13A and 13B are received in the sync-detecting and error-correcting circuits 14A and 14B which, in turn, detect respectively synchronous signals SYNC and identification signals ID from the received signals Vl4 and Vl5 and remove error components included in the recorded data. Resultant signals Vl6 and Vl7 from the sync-detecting and error-correcting circuits 14A and 14B are applied to the deinterleaving circuit 15A and 15B which, in turn, deinterleave the signals Vl6 and V17 to the original signal forms, respectively. Resultant signals Vl8 and Vl9 are then sent to the deformatter 16 of the frame removing unit 35.

At this time, the frame position information detecting unit 33 detects index information recorded on a control track disposed at the lower edge of the magnetic tape by the index head 31. The index information is a pulse indicative of a track including an I-frame. On the other hand, the recording position-synchronized block detector 40 detects recording position-synchronized blocks recorded with I-frames from the outputs Vl6 and Vl7 of the sync-detecting and error-correcting circuits 14A and 14B. Upon detecting the index information in order to achieve a discrimination for the position of a specific track, the index signal detector 36 takes into consideration the time taken to control a speed matched with a speed multiple and calculated in the capstan servo speed calculator 38 of the tape Speed controlling unit 34. The physical position of the index head 31 is determined by the processing speed of the capstan servo speed calculator 38.

The recording position-synchronized block detector 40 also detects the outputs VL6 and Vl7 of the sync-detecting and error-correcting circuits 14A and 14B and separates recording position-synchronized blocks shown in Figure 11 from the detected signals Vl6 and Vl7. The recording position-synchronized block detector 40 outputs a signal 40 which is indicative of codes relating to the speed multiple and selected from codes indicative of relative positions and present in the separated synchronous blocks.

The recording position decoder 39 decodes the signal V40 received from the recording position-synchronized block detector 40 and the speed multiple n. An optional code DIFi present in each synchronous block is a code indicative of the number of tracks present between the current track and the i-th track including specific data recorded.

Accordingly, the frame position information detecting unit 33 detects specific track position information periodically or non-periodically recorded and track position-information about I-frames recorded in the recording position-synchronized blocks, taking into consideration the calculation time taken to control the speed of the capstan motor M2 and the driving time. In this connection, the capstan servo speed calculator 38 receives the position information V36 from the index signal detector 36 and the position information V39 from the recording position decoder 39 and thereby calculates the rotation speed of the capstan motor M2 in accordance with the input speed multiple n. Resultant signal V38 from the capstan servo speed calculator 38 is then applied to the capstan servo driving signal generator 37 which, in turn, controls the speed of the capstan motor M2 so that the capstan motor M2 can be driven repeatedly at a normal speed and a high speed. As a result, the pleads HD1 to HD4 mounted on the drum 6 performs repeatedly a travel at the normal speed on specific tracks of the magnetic tape and a jumping travel on other tracks, thereby enabling reproduction of speed-varied videos.

Figures 13A to 13C illustrate an example of a capstan servo speed control in a case where speed-varied specific data have been recorded on every two-track at intervals of four tracks. In this case, the capstan motor M2 is driven two tracks at a normal speed in the same direction as the recording tracks for first half of the initial cycle shown in Figure 13B. For next half of the initial cycle, the capstan motor M2 is driven four tracks at a high speed. During the accelerated driving, the capstan motor M2 exhibits the driving characteristic shown in Figure l3A because the output V37 of the capstan servo driving

signal generator 37 is periodically varied in level, as shown in Figure 13C. By virtue of such a speed-varied driving of the capstan motor M2, therefore, it is possible to reduce an excessive characteristic of the capstan servo speed.

The outputs Vl8 and Vl9 from the digital reproduction unit 32 resulted from the speed-varied reproduction are sent to the deformatter 16 of the frame removing unit 35, converted into the signal form prior to the recording, and then outputted as a speed-varied reproduced signal V0 such as a digital HDTV signal or a normal TV signal via the interface 17.

For the signal conversion in the deformatter 16, it is required to remove the stuffing bits or dummy bits added for preventing the underflow phenomenon of the frame memory 23 upon recording data for varied speed on specific tracks. To this end, the stuffing bit-detecting · and removing circuit 42 supplies a bit removing signal V42 for preventing any bit string from being outputted to the interface 17 when a stuffing synchronous code recorded at the starting portion of stuffing bits is detected. The supplying of the bit removing signal V42 is continued until a stuffing bit end code is detected.

In the reproduction at the normal speed, the frame removing unit 35 also separates data of recording tracks for varied speed so that the I-frame data recorded on the magnetic tape for the speed-varied reproduction is prevented from being outputted to the interface 17 and thereby being included in the reproduced signal V0. On the other hand, the frame removal timing generator 41 receives position information of tracks recorded with specific data for speed-varied from both the recording position decoder 39 and the index signal detector 36 of the frame position information detecting unit 33. Based on the output SWP of the drum pulse generator 7 shown in Figure 14A, the frame removal timing generator 41 then outputs a frame removing signal V4l shown is in

Figure 14C to the deformatter 16.

Based on the frame removing signal V41, the deformatter 16 removes I-frame data from the signals V18 and V19 (Figure 14B) received from the deinterleaving circuits 15A and 15B of the digital reproduction unit 32. As a result, the deformatter 16 output a signal V20 shown in Figure 14D, thereby enabling the reproduction at the normal speed.

As apparent from the above description, the present invention provides a circuit for controlling recording and reproduction in a digital cassette tape recorder capable of separating specific data for speed-varied reproduction from compressed digital video signals and recording them on designated tracks in a recording mode, recording position information of the designated tracks on a control track by an index head or recording position information of recording position-synchronized blocks at the starting portions of the designated tracks recorded with the specific data so as to accurately scan the designate tracks in a reproduction mode, controlling a capstan servo speed so as to maintain the travel of a magnetic tape at a normal speed and periodically or non-periodically accelerate or decelerate it where specific data for varied-speed have been recorded periodically or non-periodically on predetermined portions of tracks, thereby making heads travel repeatedly at the normal speed and the high speed and thereby detect continuously the specific tracks for varied speed. Also, the specific data for speed-varied reproduction is removed in the reproduction at the normal speed. Thus, the reproduction at the normal speed can be accomplished.

Accordingly, the present invention provides a repeatability of reproduced video at a varied speed without any deterioration in picture quality in that it enables recording of specific data for speed-varied reproduction and continuous detection of the specific data in the speed-varied reproduction.

As so far described, the elevator durability evaluating apparatus and method according to the present invention are directed to preventing accidents of the elevator and